REMARKS

Claims 1-20 are pending in the application. Claims 1-4 and 16-20 are withdrawn. Claim 5 is amended herein. Reconsideration and allowance of claims 5-15 are respectfully requested.

Rejection Under 35 U.S.C. § 112

Claims 5-15 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. According to the office action, step (d) refers to removal of the second insulation layer and the charge storage layer, and step g) refers to removal of the second insulation layer and the charge storage layer. The first and second removal are alleged to render the claim indefinite.

In order to improve the clarity of the claimed subject matter, claim 5 has been amended. Specifically, step (d) has been amended to refer to "a first portion of the second insulation layer (4) and a first portion of the charge storage layer (3)." Step g) has been amended to refer to "removal of a second portion of the second insulation layer (4), [and] a second portion of the charge storage layer (3)." Support for this amendment is found in the application as filed, such as FIG. 3C and FIG. 3D, so that no new matter is added by this amendment. As is clearly illustrated by the drawing, different portions of the structure are removed to define particular structural features, such as the islands defining memory locations LB and RB.

In light of the amendments to independent claim 5, it is respectfully submitted that this claim defined the recited subject matter with the specificity and definiteness required by 35 U.S.C. § 112, second paragraph. Accordingly, withdrawal of the rejection of claims 5-15 under 35 U.S.C. § 112 is respectfully requested.

Rejection Under 35 U.S.C. § 103(a)

Claims 5-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent number 6,011,725 to Eitan ("Eitan") in view of U.S. patent no. 5,963,480 to Harari ("Harari"). Reconsideration is respectfully requested.

Independent claim 5 has been amended to more clearly define the subject matter defined by this claim. Specifically, claim 5 has been amended to better define the portions of the second insulation layer (4), the charge storage layer (3) and the first insulation layer (2) being removed during steps of the claimed method. During step d), a first portion of the second insulation layer (4) and a first portion of the charge storage layer (3) are removed, corresponding to FIG. 3C. During step g), a second portion of the second insulation layer (4), a second portion of the charge storage layer (3) and a first portion of the first insulation layer (2) are removed. Then during step l), a third portion of the second insulation layer (4), a third portion of the charge storage layer (3) and a second portion of the first insulation layer (2) are removed. This selective patterning is done "in order for form locally delimited memory locations (LB, RB)." This is a unique feature of the claimed invention.

The present application illustrates a conventional memory cell, such as Eitan and Harari teach, in FIG. 1. The charge storage layer (labeled 3 in FIG. 1) is continuous between the two memory areas LB and RB. However, this conventional shape permits a charge shift within the charge storage layer. This in turn leads to threshold voltage shifts and read current changes, as explained in paragraph [0010] of US patent publication no. US 2005/0121714 for the present application. The conventional nonvolatile memory cell is limited by these disadvantages.

The nonvolatile memory cell with delimited memory locations (LB, RB) provides significant operational advantages over previous devices. This is explained in paragraph [0027] of the published application:

> In contrast to the conventional semiconductor memory cell, however, the electrically non-conductive charge storage layer 3 is now not connected together in a continuous manner, but rather is interrupted. By virtue of this interruption or gap U in the electrically non-conductive charge storage layer 3, a first locally

> delimited memory location LB on the source side and a second locally delimited memory location RB on the drain side are formed in a completely isolated manner, as a result of which the drift and diffusion processes described in the introduction cannot lead to a loss of data. The charge density in the locally delimited memory locations LB and RB thus remains unchanged, for which reason outstanding charge retention properties are obtained.

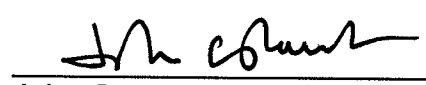
Thus, an important structural key to these advantages is the interrupted charge storage layer (3). By removing the portion of the charge storage layer (3) between the memory locations LB, RB, the memory locations LB, RB are locally delineated memory locations. That is, each memory location LB, RB, is isolated from the other memory location. The disadvantages of the conventional cell in Eitan and Harari can not affect the memory cell defined by claim 1.

Moreover, the cited references fail to show the unique structural features of claim 5. Eitan shows in FIG. 2 a charge trapping layer 20 which extends over the entire channel region, from source to drain. Harari is similar. For example, Harari FIG. 6b shows a continuous charge storage layer 504a. Thus, like the conventional memory cell described in the background section of the application, the charge storing layer in the two applied references is connected together in a continuous manner.

Accordingly, independent claim 5 includes limitations absent from the cited references and is therefore novel and unobvious over these references. Therefore, withdrawal of the rejections of claims 5-15 is respectfully requested. Claims 6-15 are dependent from claim 5 and are allowable for the same reasons.

With this response, the application is believed to be in condition for early action on the merits. Should the examiner deem a telephone conference to be of assistance in advancing the application to allowance, the examiner is invited to call the undersigned attorney at the telephone number below.

Respectfully submitted,



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